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SPECIFICATION

1. TITLE OF THE INVENTION

MANUFACTURING METHOD OF MATRIX DISPLAY PANEL

2. CLAIMS

[Claim 1] A manufacturing method of a matrix display panel comprising the steps of:

(1) setting a gate electrode forming a first electrode on an insulating substrate;

(2) setting a gate insulating layer in a region except in a terminal pickup portion in a peripheral portion of said insulating substrate;

(3) setting a semiconductor layer on said gate insulating layer approximately in a same shape as said gate insulating layer;

(4) setting a protection insulating layer approximately in a same shape as said semiconductor layer;

(5) setting source and drain contact holes in said protection insulating layer;

(6) setting a second electrode film approximately over a whole surface of a surface including said protection insulating layer;

(7) patterning said second electrode film in a shape of source

and drain electrodes;

(8) setting an interlayer insulating layer in a surface including said source and drain electrodes;

(9) setting a picture element contact hole in said interlayer insulating layer;

(10) setting a third electrode film in a surface including said interlayer insulating layer;

(11) pattering said third insulating film in a shape of a picture element electrode; and

(12) sandwiching a displaying medium between a surface having the picture element electrode of said substrate and a transparent common electrode provided on a transparent insulating substrate.

[Claim 2] A manufacturing method of a matrix display panel as claimed in claim 1, wherein an accumulated capacity forming electrode is provided other than the gate electrode in the first step, and an accumulated capacity is formed between the accumulated capacity forming electrode and the drain electrode provided in the seventh step.

3. DETAILED DESCRIPTION OF THE INVENTION

Field of Industrial Application

The present invention relates to a manufacturing method of a reflection type matrix display panel in which a picture element effective area is enlarged.

[Structure of Prior Art and Problems thereof]

In order to matrix display a liquid crystal or the like at a low duty ratio, there is an attempt that a switch element constituted by a thin film transistor (hereinafter, referred

to as TFT) is introduced to each of the picture elements. In other words, as shown in a plan view in Fig. 1 and a cross sectional view along line A-A' in Fig. 2, a TFT substrate 10 with a TFT array is structured such that a gate electrode 1, a gate insulating film 2, a semiconductor layer 3, a drain electrode 4, a source electrode 5 and a picture element electrode 8 are configured on an insulating substrate 7 such as a glass or the like as each of element units. The drain electrode 4 is connected to the picture element electrode 8 via a contact hole 9 provided in the gate insulating layer 2.

As shown in Fig. 3, an X-Y matrix display panel capable of displaying a large number of picture elements can be configured by sandwiching a display medium 12 such as a liquid crystal or the like between the substrate 10 with the TFT array in Fig. 1, and a substrate having a transparent common electrode 13 such as an indium oxide, a tin oxide or the like on a transparent insulating substrate such as a glass or the like.

Showing an electric equivalent circuit of the matrix display panel with a TFT array as shown in Figs. 1 to 3, it becomes as shown in Fig. 4. A description will be given below of a principle of operation based on Figs. 1, 2 and 4.

As a matter of convenience, a TFT 11 is considered as an n-channel enhancement type using CdSe or an amorphous silicon as a semiconductor layer. In this case, at a time of keeping the gate electrode 1 at a potential equal to or lower than that of the source electrode 5 in a state of applying a voltage so as to set the drain electrode 4 positive to the source electrode 5, the TFT 11 comes to an off state, and a current hardly flows between the source and the drain. However, if the gate electrode

1 is kept positive with respect to the source electrode 5, electrons are induced into the semiconductor film which comes into contact with the gate insulating film. As a result, the TFT 11 comes to an on state, and the current flows between the source and the drain. In a case of matrix driving, a signal is applied sequentially to normal lines. For example, Figs. 5(a) and (b) show an example of carrying out an AC drive by using the liquid crystal for the display medium. Voltage waveforms of a scanning side (Y1 to Y3) and a signal side (X1 to X3) in the case of carrying out 3 × 3 dot matrix display shown in Fig. 5(b) are shown in Fig. 5(a), and an ON-cell is shown by a diagonal line in Fig. 5(b).

In the conventional matrix display panel with the TFT array, as is apparent from Fig. 1, the region of the source 5 and the gate 1 is a display impossible region, and only a region except the contact portion of the picture element electrode 8 can substantially contribute to the display. In other words, the picture element effective area is significantly deteriorated due to the source electrode 5 and the gate electrode 1. Particularly, a high picture element density can not similarly reduce a pattern in Fig. 1. This is because a wiring resistance is increased based on a narrow width of the source and gate electrodes, whereby a signal waveform is deformed and a defect of disconnection tends to be generated. This causes a further reduction of a rate of the picture element effective area, and the electrode structure as shown in Fig. 1 drops down a display quality particularly in a high resolution display and it is a severe problem to cause a reduction of a macroscopic contract.

Object of the Invention

The present invention provides a manufacturing method of a matrix display panel which intends to enlarge a picture element effective area while improving an array manufacturing process and employing a simplified process, for the purpose of overcoming the conventional problems as mentioned above.

Structure of the Invention

A manufacturing method in accordance with the present invention includes the steps of (1) setting a gate electrode forming a first electrode on an insulating substrate, (2) setting a gate insulating layer in a region except a terminal pickup portion in a peripheral portion of the insulating substrate, (3) setting a semiconductor layer on the gate insulating layer approximately in a same shape as the gate insulating layer, (4) setting a protection insulating layer approximately in a same shape as the semiconductor layer, (5) setting source and drain contact holes in the protection insulating layer, (6) setting a second electrode film approximately over a whole surface of a surface including the protection insulating layer, (7) patterning the second electrode film in a shape of source and drain electrodes, (8) setting an interlayer insulating layer in a surface including the source and drain electrodes, (9) setting a picture element contact hole in the interlayer insulating layer, (10) setting a third electrode film in a surface including the interlayer insulating layer, (11) pattering the third insulating film in a shape of a picture element electrode, and (12) sandwiching a displaying medium between a surface having the picture element electrode of the substrate and a transparent common electrode provided on a

transparent insulating substrate.

In the present invention, since a structure is made such that the semiconductor layer is used in a state of a continuous phase without being made small, it is possible to enlarge the picture element effective area, and it is possible to dissolve an increase of the steps, a dispersion of an element characteristic in the steps and a reduction of a yield ratio, which corresponds to the defect in the conventional method of sectioning the semiconductor layer into small parts, and setting the semiconductor layer in the small part.

Description of Embodiments

Hereinafter, an embodiment of the present invention will be described with reference to the accompanying drawings.

According to a manufacturing method of the present invention, first, a gate electrode material such as a chrome, a nichrome, a molybdenum, a gold or the like is formed on an insulating substrate such as a glass or the like, and then patterned in a gate electrode 1 shape as shown in a plan view in Fig. 6(a) and a cross sectional view along line B-B' in Fig. 6(b) by using a first photomask. (Generally, a common electrode terminal 13 is provided for picking up a common electrode 13 onto an identical substrate 7, however, an illustration is omitted in the following drawings.) Next, in a case of manufacturing an amorphous silicon TFT, for example, in accordance with a plasma CVD method, as shown in Figs. 7(a) and (b), the substrate is put within a plasma reactor, a mixed gas having a silane gas as a main component is plasma discharged, and a gate insulating film 2 of a silicon nitride or a silicon oxide is formed. At this time, in order to make a step of later

removing the film unnecessary, the plasma discharge is carried out in a state of bringing, for example, a metal mask or the like into contact with the substrate, in a peripheral portion of the substrate having the gate, in such a manner that the film is not piled up in the terminal portion 15. Next, the gas composition is changed, the plasma discharge is again carried out by using the silane gas as the component, and the amorphous silicon semiconductor film 3 is piled up in the same shape as the gate insulating film. After a protection insulating film 18 is formed from the above, source and drain contact holes 19 and 20 are provided as shown in Fig. 7 in accordance with a photo etching. Next, the second electrode film is provided approximately in a whole surface of the substrate in accordance with a vapor deposition, a sputtering or the like as shown in Figs. 8(a) and (b), and is thereafter patterned as the source electrode 5 and the drain electrode 4 shapes in accordance with a photo etching. Next, as shown in Figs. 9(a) and (b), there is provided an organic insulating film such as a photoresist, a polyimide film or the like, or an inorganic insulating film such as an alumina, a silicon dioxide, a silicon nitride or the like in accordance with a vapor deposition, a sputtering, a CVD method or the like, as an interlayer insulating film 21. The interlayer insulating film is provided with a picture element electrode contact hole 22 in accordance with a photo etching. Next, as shown in Figs. 10(a) and (b), a metal film to be the picture element electrode is formed approximately in a whole surface of the substrate mentioned above in accordance with the vapor deposition or the sputtering, and is patterned in a shape of the picture element electrode 8 in accordance with

the photo etching.

The description of the TFT manufacturing process is given above in accordance with the present invention based on the plasma CVD method, however, the same structure is applied to a case of using the different gate insulating film 2 and the semiconductor layer 3 (a cadmium selenide, a tellurium or the like), the interlayer insulating film or the like in accordance with the vapor deposition or the sputtering method.

In any case, if a display medium is sandwiched between the transparent electrode 13 of the substrate 14 of the glass, the plastic or the like having the transparent electrode and the TFT array manufactured as mentioned above, the display panel is formed.

As the display medium 12 used in the present invention, various display mediums can be used, however, particularly in a case where the picture element electrode is constituted by an opaque reflecting electrode such as an aluminum or the like, it is possible to employ a liquid crystal material used in a so-called guest host mode in which a dichroic coloring matter is dissolved in a nematic liquid crystal or a mixed liquid crystal constituted by the nematic liquid crystal and a cholesteric liquid crystal, a so-called DSM mode liquid crystal obtained by somewhat adding an ionic dopant to the nematic liquid crystal having a negative dielectric anisotropy and forming a scattering kernel by applying an electric field so as to whiten the liquid crystal, and a so-called phase transition liquid crystal obtained by generating a phase change between a nematic phase and a cholesteric phase by applying an electric field to a mixed body of the nematic liquid crystal and the cholesteric liquid

crystal, and achieving a transparent or whitened display. On the other hand, in addition to the liquid crystal, for example, it is possible to use a so-called electrophoretic displaying dispersion system obtained by dispersing a pigment particle having a different color in an organic solvent colored by a dye, an electrolytic coloring type display medium, or an electroluminescence layer.

As mentioned above, in accordance with the manufacturing method of the present invention, the source electrode 5 and the gate electrode 1 are isolated by the gate insulating layer 2, the semiconductor layer 3 and the protection insulating layer 18, and a crossover insulating characteristic is kept. Further, since the picture element electrode 8 and the source electrode 5 are isolated by the interlayer insulating layer 18, and the gate electrode 1 and the picture element electrode 8 are isolated by a large number of insulating layers and the semiconductor layers, an electric insulating characteristic is sufficiently retained. Accordingly, it is possible to make the picture element electrode 8 larger at an overlapping amount with the source electrode 5 and the gate electrode 2 than the conventional one, and it is possible to significantly improve the picture element effective area in the display panel in accordance with the present method than the conventional manufacturing method.

In the present invention, a description will be given below of an improved structure which further improves a performance of the TFT array.

In other words, instead of setting only the gate electrode on the substrate prior to the formation of the gate insulating film, a parallel capacity forming common electrode 17 is

simultaneously formed as shown in Fig. 11. This can be achieved by simply changing the pattern of the photo mask as shown in Fig. 11 without increasing the steps. The TFT array is formed sequentially in accordance with the identical process as mentioned first.

The parallel capacity forming common electrode 17 is electrically connected to the common transparent electrode 13 sandwiching the display medium 12 before or after sandwiching the display medium 12, whereby the panel is finished. In this case, the gate insulating layer 2, the semiconductor layer 3 and the interlayer insulating layer 18 are sandwiched in a form of a lamination between the parallel capacity forming common electrode 17 and the picture element electrode 8, thereby forming a capacitor. Further, since the parallel capacity forming common electrode and the common transparent electrode are electrically connected, the capacity is applied in parallel electrically to the picture element capacity formed therein, and is named as the parallel capacity.

In a case where the picture element parallel capacity is applied to the TFT array, there can be generated an advantage that it is possible to use a low resistance display medium, it is possible to drive in a low voltage, and it is possible to use the TFT having a comparatively low off resistance.

In the process in accordance with the present invention mentioned in Figs. 6 to 10, the present array forming method particularly has a high practical value, in a point that the advantage as mentioned above can be easily generated without particularly adding any process.

[Effect of the Invention]

An important thing in the present invention is as follows. There has been conventionally employed the method of setting the semiconductor layer in the whole surface at a time of forming the TFT array and thereafter dividing into the small parts with the photo etching, or previously forming the semiconductor only in the small parts by using the vapor deposition mask or the like. On the contrary, the present invention pays attention to the point that one step is increased, the element characteristic is dispersed and the yield ratio reduction tends to be caused, in the method of sectioning the semiconductor layer into the small parts or setting the semiconductor layer in the small parts, and employs the structure using the semiconductor layer in the continuous phase state without making the semiconductor layer small. Accordingly, there is employed the method of applying the shielding mask only to the region for picking up the electrode terminal at a time of forming the insulating layer and the semiconductor layer in such a manner as to prevent the insulating layer and the semiconductor layer from being formed in this region. Therefore, it is possible to prevent the film formation in the unnecessary portion without increasing the step.

On the other hand, since the protection insulating layer 18 is provided on the channel region 16 (Fig. 8) of the TFT, and the semiconductor layer 3 is protected without directly coming into contact with the display medium 12, it is a great advantage that the stable TFT can be obtained for a long term.

As a further important advantage of the present invention, it is possible to securely shield light to the TFT channel portion 16. In general, the TFT semiconductor film 3 such as the

amorphous silicon, the cadmium selenide or the like has a photoconductivity and the characteristic is changed in accordance with a peripheral brightness, however, in the structure in accordance with the present invention, since the opaque picture element electrode covers the channel portion of the TFT, and has the light shielding effect, it is possible to use under a stable characteristic.

4. BRIEF DESCROPTION OF THE DRAWINGS

Fig. 1 is an enlarged plan view of a main part of a conventional TFT array for a matrix display panel;

Fig. 2 is a cross sectional view along line A-A' in Fig. 1;

Fig. 3 is a cross sectional view of a matrix display panel with a TFT array;

Fig. 4 is a circuit diagram of an electric equivalent circuit of the matrix display panel with the TFT array in Fig. 3;

Figs. 5(a) and (b) are a waveform view and a schematic view explaining a driving of each of cells of the matrix display panel;

Figs. 6(a) to 10(b) are plan views of a main part for explaining each of steps of a manufacturing method in accordance with the present invention and cross sectional views along line B-B';

and

Fig. 11 is a partially-cut plan view of a TFT array forming a substrate used in a further improved manufacturing method in accordance with the present invention.

1 Gate electrode

2 Gate insulating layer

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3	Semiconductor layer
4	Drain electrode
5	Source electrode
7	Substrate
8	Picture element electrode
13	Transparent common electrode
14	Glass substrate
15	Terminal
16	TFT channel region
17	Parallel capacity forming common electrode
18	Protection insulating layer
19	Drain contact hole
20	Source contact hole
21	Interlayer insulating layer
22	Picture element contact hole

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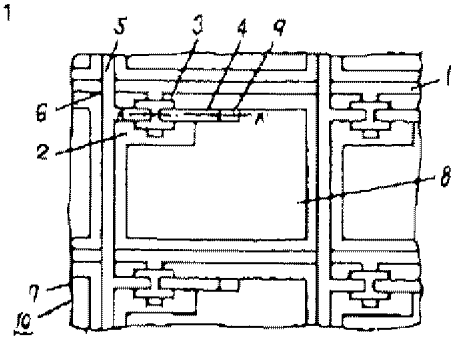
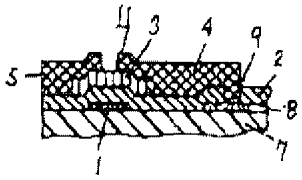
[Fig. 1]

Fig. 1



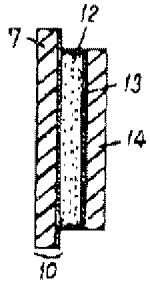
[Fig. 2]

Fig. 2



[Fig. 3]

Fig. 3



[Fig. 4]

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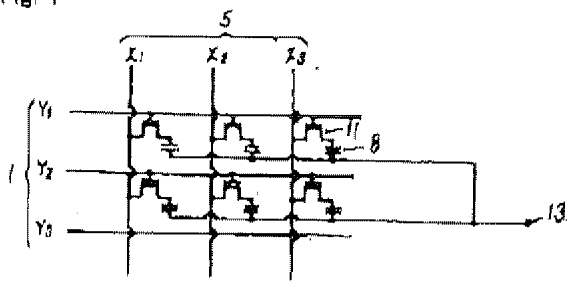
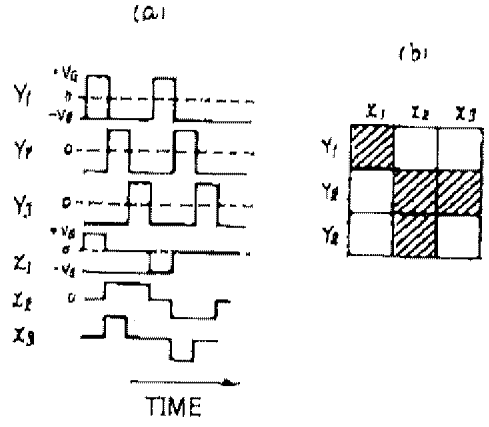
Fig. 4



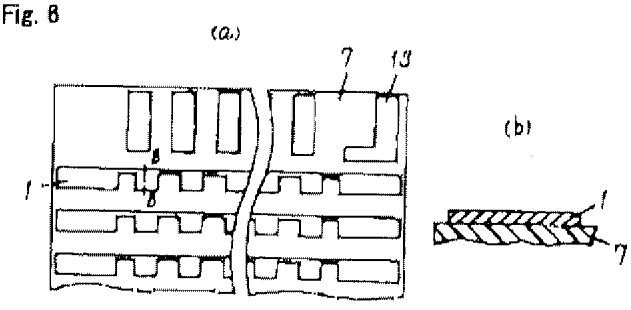
[Fig. 5]

FIG. 5



[Fig. 6]

Fig. 6



[Fig. 7]

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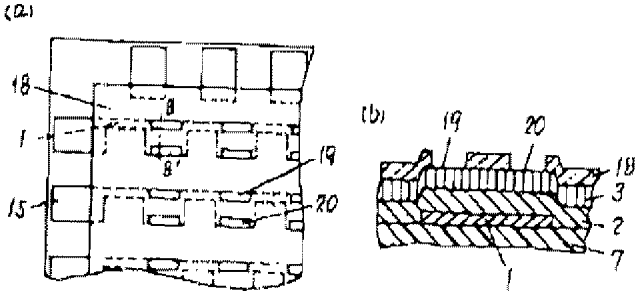
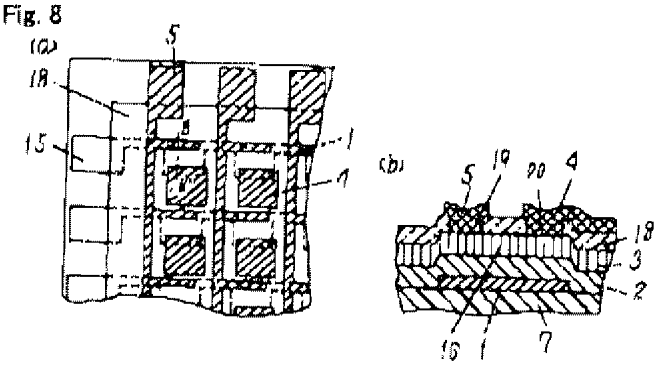
Fig. 7



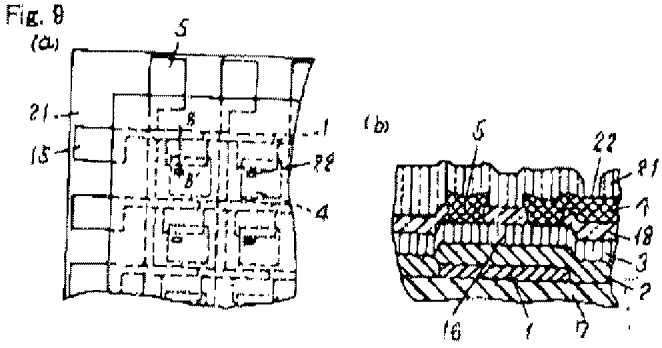
[Fig. 8]

Fig. 8



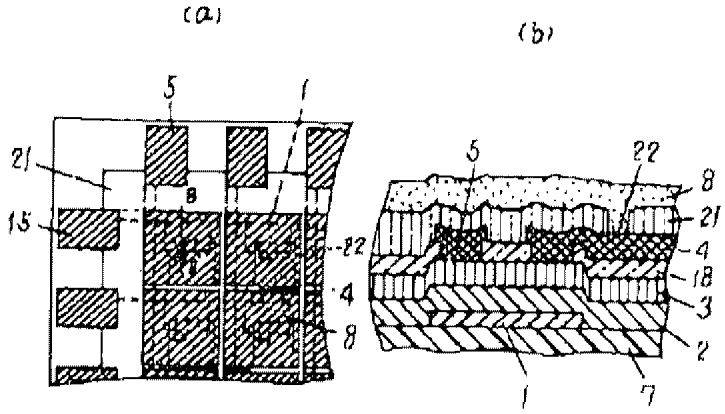
[Fig. 9]

Fig. 8



[Fig. 10]

Fig. 10



[Fig. 11]

Fig. 11